WHAT IS CLAIMED IS:

1. A method of operating a memory circuit, comprising the steps of:

applying a first voltage to a power terminal of a memory cell having a first and a second data terminal;

storing a data bit in the memory cell while the power terminal receives the first voltage;

applying a second voltage different from the first voltage to the power terminal;

applying a third voltage to the first and second data terminals while the power terminal receives the second voltage; and

applying the first voltage to the power terminal.

2. A method as in claim 1, comprising the step of removing the third voltage from the first and second data terminals.

3. A method as in claim 1, wherein the step of applying the third voltage comprises activating a wordline.

4. A method as in claim 3, wherein the step of applying the third voltage comprises activating a control signal.

5. A method as in claim 1, comprising the steps of:

detecting a control signal at the memory circuit;

waiting for a grace period after the step of detecting; and

applying the second voltage and the third voltage in response to the step of waiting.

6. A method as in claim 5, wherein the grace period is determined by counting a predetermined number of clock cycles.

7. A method as in claim 1, comprising the steps of:

detecting a control signal at the memory circuit; and

applying the second voltage and the third voltage in response to the step of detecting.

8. A memory circuit, comprising:

an array of memory cells arranged in rows and columns, each memory cell having a power terminal, a control terminal, a first data terminal, and a second data terminal;

a plurality of bitline pairs, each bitline pair coupled to respective first and second data terminals of each memory cell in a respective column of memory cells.

a plurality of wordlines, each wordline coupled to a control terminal of a respective row of memory cells;

a row counter circuit coupled to receive a clock signal, the row counter circuit producing a sequence of row address signals in synchronization with the clock signal and in response to a control signal; and

a row decoder circuit coupled to a plurality of wordlines and coupled to receive the sequence of row address signals.

9. A memory circuit as in claim 8, comprising a clock counter circuit coupled to receive the clock signal, the clock counter circuit producing the control signal after a grace period.

10. A memory circuit as in claim 9, wherein the grace period corresponds to a number of clock cycles.

11. A memory circuit as in claim 8, wherein a processor produces the control signal after a grace period.

12. A method of operating an electronic device, comprising the steps of:

applying a first voltage to a first part of the electronic device;

applying a second voltage to a second part of the electronic device;

changing the first voltage to a third voltage different from the first voltage while maintaining the second voltage;

applying a fourth voltage to the first part of the electronic device while maintaining the second voltage;

removing the fourth voltage from the first part of the electronic device; and

changing the third voltage to the first voltage while maintaining the second voltage.

13. A method as in claim 12, wherein the first voltage is equal to the second voltage.

14. A method as in claim 12, wherein the first voltage is a power supply voltage and the third voltage is ground.

15. A method as in claim 12, wherein the first part of the electronic device is a memory array and the second part of the electronic device is a peripheral circuit.

16. A method as in claim 12, comprising the steps of:

detecting a control signal at the electronic device;

waiting for a grace period after the step of detecting; and

changing the first voltage to the third voltage in response to the step of waiting.

17. A method as in claim 16, wherein the grace period is determined by counting a predetermined number of clock cycles.

18. A method as in claim 12, comprising the steps of:

detecting a control signal at the electronic device; and

changing the first voltage to the third voltage in response to the step of detecting.

19. A method as in claim 12, wherein the electronic device is a wireless telephone handset.

20. A method as in claim 12, wherein the electronic device is a computer.

21. A method as in claim 12, wherein the electronic device is a video game.

22. A method as in claim 12, wherein the first voltage is an array supply voltage and wherein the first part is a memory array.

23. A method as in claim 12, wherein the second voltage is a peripheral supply voltage and wherein the second part is a peripheral circuit.

24. A method as in claim 23, wherein the peripheral circuit is a row decoder circuit.

25. A method as in claim 12, wherein the third voltage is ground.

26. A method as in claim 12, wherein the fourth voltage is a precharge voltage.

27. A method as in claim 12, wherein the step of applying the fourth voltage comprises activating a wordline and wherein the step of removing the fourth voltage comprises inactivating the wordline.